AMENDMENTS TO THE CLAIMS

1. (Currently amended) A semiconductor apparatus, comprising:

a semiconductor substrate;

an electrode pad comprising a metal layer and formed over the semiconductor substrate, said electrode pad providing contact between said semiconductor apparatus and external circuitry;

a MOS transistor formed over the semiconductor substrate; and

a circuit formed over said semiconductor substrate and in a region under the electrode pad, said circuit comprising an array ~~plurality~~ of adjacent resistive elements formed of a semiconductor material, said electrode pad being formed over said array ~~plurality~~ of resistive elements such that said electrode pad extends transversely across said array.

2. (Previously presented) The semiconductor apparatus according to Claim 1, wherein the resistive elements comprise a material selected from the group consisting of polysilicon, silicon germanium, and silicon chrome.

3. (Previously presented) The semiconductor apparatus according to Claim 1, wherein the resistive elements include a plurality of resistors connected serially.

4. (Previously presented) The semiconductor apparatus according to Claim 1, wherein the MOS transistor comprises a gate electrode comprises a material selected from the group consisting of polysilicon, silicon germanium, and silicon chrome.

5. (Previously presented) The semiconductor apparatus according to Claim 1, further comprising:

an insulating film formed on the semiconductor substrate in a region in a vicinity of the electrode pad; and

a fuse element formed on the insulating film, said fuse element in electrical contact with said plurality of resistive elements.

6. (Previously presented) The semiconductor apparatus according to Claim 5, wherein the fuse element comprises a material selected from the group consisting of polysilicon, silicon germanium, and silicon chrome.

7. (Previously presented) The semiconductor apparatus according to Claim 5, further comprising:

a rerouting layer formed in a region above the fuse element; and

an external connection terminal formed on the rerouting layer in a region different from a formation region of the electrode pad.

8. (Previously presented) The semiconductor apparatus according to Claim 5, wherein the circuit comprises a voltage setting circuit, the resistive elements comprise at least two resistors for producing a split voltage based on an input source power voltage, and the voltage setting circuit changes the split voltage according to a condition of the fuse element.

9. (Previously presented) The semiconductor apparatus according to Claim 1, wherein the resistive elements comprise at least two resistors for producing a split voltage based on an input source power voltage, the circuit comprises a reference voltage generator for generating a reference voltage and a voltage detector including a comparator for performing a comparison of the split voltage with the reference voltage.

10. (Previously presented) The semiconductor apparatus according to Claim 9, wherein the circuit further comprises an output driver for controlling an output voltage based on an input voltage, and the comparator of the voltage detector outputs a gate control voltage as a result of the comparison for controlling the output driver to control the output voltage.

11. – 16. (Canceled)

17. (Previously presented) The semiconductor apparatus according to Claim 1, wherein the resistive elements include a plurality of doped semiconductor material resistors.

18. (Previously presented) The semiconductor apparatus according to Claim 4, wherein said gate electrode has lengthwise ends which are bent in an upward direction over an insulating film.

19. (Currently amended) A semiconductor apparatus, comprising:

a semiconductor substrate;

an oxide film formed over the semiconductor substrate, the oxide film comprising a resistive-element formation region, a fuse-element formation region, and a MOS transistor formation region, the resistive-element formation region having a circuit comprising an array of strip-shaped resistive elements formed of a semiconductor material;

an insulating layer formed over the oxide film and having an electrode-pad formation region,

wherein the electrode-pad formation region is formed over the resistive-element formation region, and wherein the electrode-pad formation region has an electrode pad

comprising a metal layer and wherein the electrode pad extends transversely across the array of strip-shaped resistive elements.

20. (Previously presented) The semiconductor apparatus of claim 19, wherein a respective low-resistance polysilicon region is formed immediately next to the lengthwise ends of each of the plurality of resistive elements.

21. (Previously presented) The semiconductor apparatus of claim 19, wherein the MOS transistor formation region includes a MOS transistor comprising a gate electrode formed of a material comprising polysilicon, the gate electrode having lengthwise ends which are bent in an upward direction over the oxide film.